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# Efficient Design of Ripple Carry Adder and Carry Skip Adder with Low Quantum Cost and Low Power Consumption

Nidhi*, Gurinderpal Singh**
*(Department of Electronics and Communication Engineering, Chandigarh University, Gharuan)
** (Department of Electronics and Communication Engineering, Chandigarh University, Gharuan)

**ABSTRACT**
The addition of two binary numbers is the important and most frequently used arithmetic process on microprocessors, digital signal processors (DSP), and data-processing application-specific integrated circuits (ASIC). Therefore, binary adders are critical structure blocks in very large-scale integrated (VLSI) circuits. Their effective application is not trivial because a costly carry spread operation involving all operand bits has to be achieved. Many different circuit constructions for binary addition have been planned over the last decades, covering a wide range of presentation characteristics. In today era, reversibility has become essential part of digital world to make digital circuits more efficient. In this paper, we have proposed a new method to reduce quantum cost for ripple carry adder and carry skip adder. The results are simulated in Xilinx by using VHDL language.

***Keywords*** **–** Carry Skip Adder, Ripple Carry Adder, Quantum Cost, Reversible Logic, VLSI

## I. INTRODUCTION

Reversible logic performs all operations in an invertible manner that marks a promising new direction. As compared with traditional logic, all computations can be reverted (i.e. the inputs can be obtained from the outputs *and* vice versa) by using reversible logic. This reversibility plays significant role for emerging technologies that may replace or at least enhance the traditional computer chip efficiency. Power dissipation and heat generation is a serious problem for today's computer chips. The non-ideal behavior of transistors and some other materials becomes primary cause for the power dissipation. A more fundamental reason for power dissipation arises from the observations made by Landauer in 1961. Landauer proved that using traditional (irreversible) logic gates always lead to energy dissipation. More precisely, exactly $kT\log_2$ Joule of energy is dissipated for each "lost" bit of information during the irreversible operation (where $k$ is the Boltzmann constant and $T$ is the temperature). [1][9]

Quantum Computation and Quantum Information can be accomplished using Quantum mechanical systems and is the study of the information processing tasks. Quantum mechanics is a mathematical schema or set of rules for the construction of physical theories. Quantum

Computation directed us to think physically about computation, and this approach turnouts many new and exciting capabilities for information processing and communication. [6]

Reversibility in computing signifies that no information about the computational states can ever be lost, so it can be recovered at any earlier stage by computing backwards or uncomputing the results. This is termed as logical reversibility. Reversible computing will also lead to improvement in power efficiency. Power efficiency will fundamentally affect the speed of circuits such as nanocircuits— and therefore the speed of most computing applications. [9]

### QUANTUM COST

Quantum Cost of the circuit is considered by knowing the number of simple reversible gates (gates of which rate is previously identified) needed to realize the circuit.

### GARBAGE OUTPUT

The output of the reversible gate that is not used as a main output or as input to other gates is called the garbage output. In little the unexploited output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are required in the circuit to retain the reversibility concept. [9]

## II. LITERATURE SURVEY

**F. J. Chih et al** [4] described that adders are fundamental building blocks and often constitute part of the critical path. In this paper, they proposed four high-speed ripple carry adder designs using the dynamic circuit techniques. The SPICE simulation shows that the proposed dynamic ripple carry adders are at least two times faster than the conventional static ripple carry adder. **T. Himanshu et al** [7] described that the reversible logic has emerged as a promising technology having its applications in low

power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. This work proposed a new $4 \times 4$ reversible gate called "TSG" gate. The proposed gate was used to design efficient adder units.

From above literature survey, it has been concluded that reversibility is essential for new technologies in terms of power efficiency. This can be done if the quantum cost and garbage output value of the digital circuits should be reduced which can only be possible by using reversible logic gates.

## REVERSIBLE LOGIC GATES [7][10]

*1) Peres Gate (PG)*

The $3 \times 3$ (Peres, 1985) is designated as follows: Input vector $I_v = (A, B, C)$ and output vector $O_v = (P = A,\ Q = A \oplus B,\ R = AB \oplus C)$. Block diagram of Peres is showed in Fig. 1. Peres gate is the combination of Feynman gate and Toffoli gate and this can contrivance operations like AND EX-OR. In this projected design PG gate is used for performing AND operation.

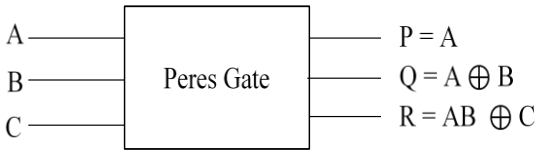


Figure 1: Peres gate

*2) Fredkin Gate (FRG)*

Input and output vectors for 3×3 FRG (Fredkin and Toffoli, 1982) is well-defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A,\ Q = \bar{A}B + AC,\ R = \bar{A}C + AB)$ FRG gate is showed in Fig. 2 and it is used in to hypothesis Multiplexers circuits. This gate is used in the planned designs for execution both AND and OR operation. This AND-OR output is attained at output R.

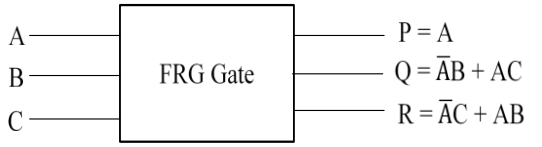


Figure 2: Fredkin gate

*3) Modified Fredkin Gate (MFRG)*

Input and output vectors for 3×3 FRG (Fredkin and Toffoli, 1982) is well-defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A,\ Q = A\bar{B} \oplus A\bar{C},\ R = \bar{A}C \oplus AB)$ MFRG gate is showed in Fig. 3 and it is used in to hypothesis in Multiplexers circuits. This gate is used in the planned designs for execution both AND and OR operation. This AND-OR output is attained at output R.

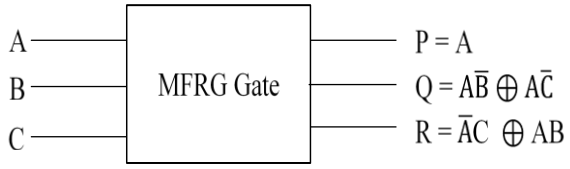


Figure 3: Modified Fredkin gate

*4) MTSG Gate*

Modified TSG (MTSG) gate is a 4×4 reversible gate with following input and output vectors, $I_v = (A, B, C, D)$ and $O_v = (P = A,\ Q = A \oplus B,\ R = A \oplus B \oplus C$ and $S = (A \oplus B).C \oplus (AB \oplus D)$. This MTSG gate in Fig. 4 can be recycled to recognize a full adder by providing constant '0' at the input D. Quantum cost of changeable MTSG gate is 6 which is lower than 13 of TSG gate. This gate is used in the enterprise so as to produce the sum, carry and the spread output of the inputs.

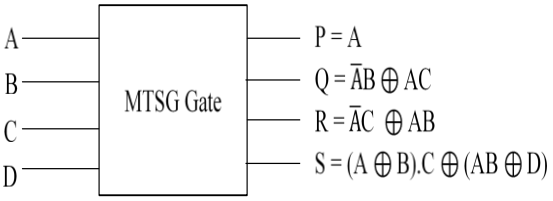


Figure 4: MTSG gate

*5) MHNG Gate*

MHNG gate is a 4x4 reversible gate with following input and output vectors, Iv = (A, B, C, D) and Ov = (P = A, Q = D, R = A⊕B⊕C, S = (A⊕B).C⊕AB⊕D). The MHNG gate is shown in Fig .5, where each output is annotated with the corresponding logic expression. One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit.

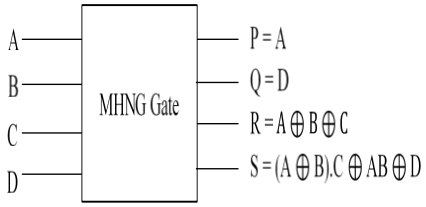


Figure 5: MHNG Gate

## III. PROPOSED WORK:

1) Ripple Carry Adder

The full adder is the simple building block in the ripple carry adder. The full adder circuit using the MTSG gate is exposed in Fig. 6. The ripple carry adder is acquired by cascading the full adders in series. The output expressions for a ripple carry adder are:

$$S_i = A \oplus B \oplus C_i$$
$$C_{i+1} = (A \oplus B).C_i \oplus AB \ (i = 0, 1, 2 \ldots .)$$

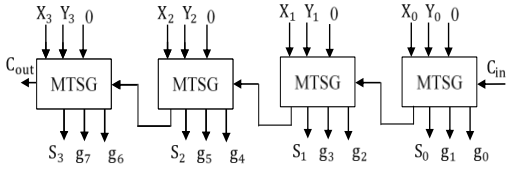


Figure 6**:** ripple carry adder using MTSG gates

The full adder circuit using the MHNG gate is exposed in Fig 7

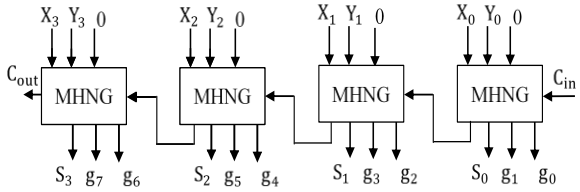


Figure 7: Ripple Carry Adder using MHNG gates

2) Carry Skip Adder

In the proposed carry skip adder, 4 bit addition is done by the modified TSG (MTSG) gates, Peres (PG) gates and Modified FRG (MFRG) gates.

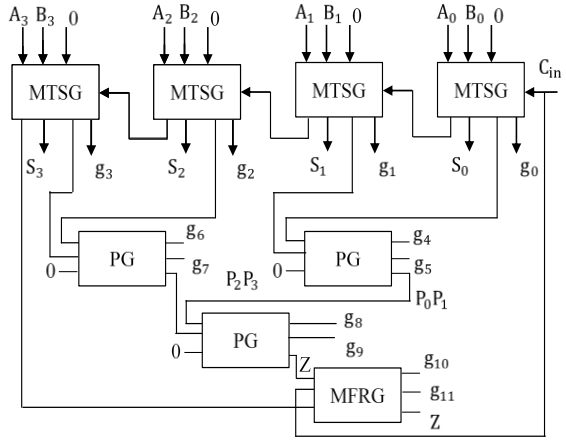


Figure 8: Carry Skip Adder using MTSG, PG and MFRG Gates

As discussed above, the ripple carry adder and carry skip adder are designed using various reversible logic gates to reduce the quantum cost and power consumption. This will increase the efficiency of digital systems. The power is calculated using XILINX power estimator.

The results of quantum cost and power consumption for ripple carry adder and carry skip adder are shown in following table.

**Table 1:** Comparison of proposed work with existing work

| **Ripple Carry Adder** | | | **Carry Skip Adder** | | |
|---|---|---|---|---|---|
| **Work** | **Quantum Cost** | **Power** | **Work** | **Quantum Cost** | **Power** |
| **Using TSG Gates [7]** | **52** | **2.404 W** | **Using MTSG, PG, FRG Gates [10]** | **41** | **2.264 W** |
| **Using MTSG Gates [proposed]** | **24** | **2.126 W** | **Using MTSG, PG, MFRG Gates [proposed]** | **40** | **1.686 W** |
| **Using MHNG Gates [proposed]** | **20** | **1.639 W** | | | |

**Table 2:** Device utilization of Ripple Carry Adder and Carry Skip Adder using different techniques

| | **RCA_TSG** | **RCA_MTSG** | **RCA_MHNG** | **CSA_MTSG** | **CSA_MFRG** |
|---|---|---|---|---|---|
| **1-bit xor2** | **12** | **16** | **16** | **24** | **24** |
| **BELS** | **12** | **12** | **8** | **16** | **16** |
| **IO Buffers** | **26** | **26** | **26** | **34** | **34** |
| **Total paths** | **63** | **55** | **51** | **133** | **133** |
| **Destination Ports** | **13** | **13** | **13** | **18** | **18** |
| **Total Delay (ns)** | **2.912** | **2.123** | **2.129** | **2.655** | **2.655** |
| **Memory Usage (kB)** | **422520** | **422272** | **446584** | **446584** | **446584** |

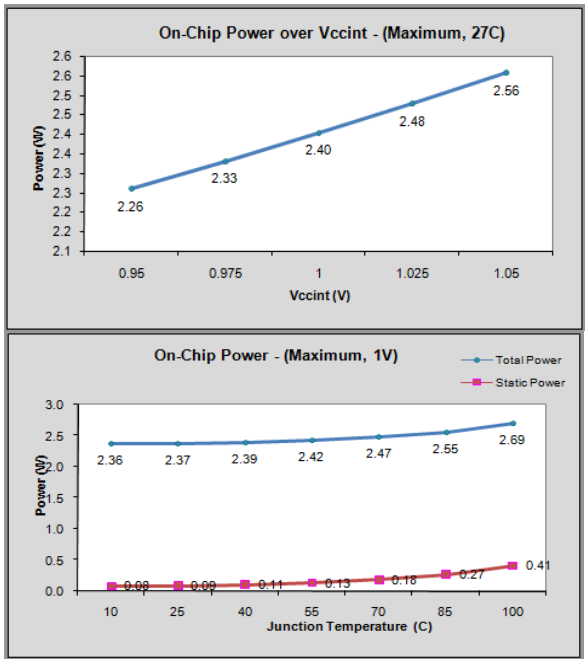


Figure 9: Power Consumption of Ripple Carry Adder using TSG Gates

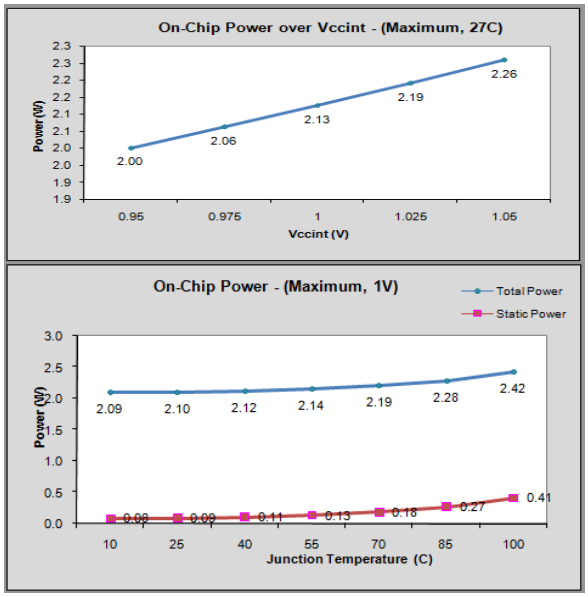


Figure 10: Power Consumption of Ripple Carry Adder using MTSG Gates

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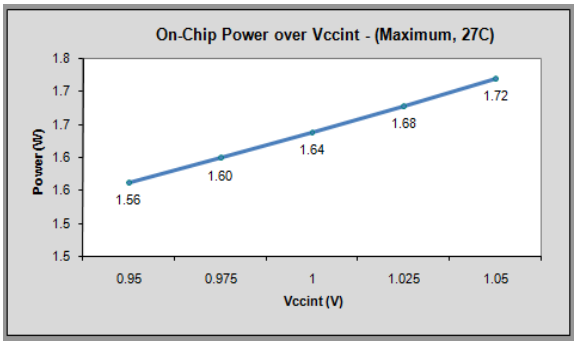


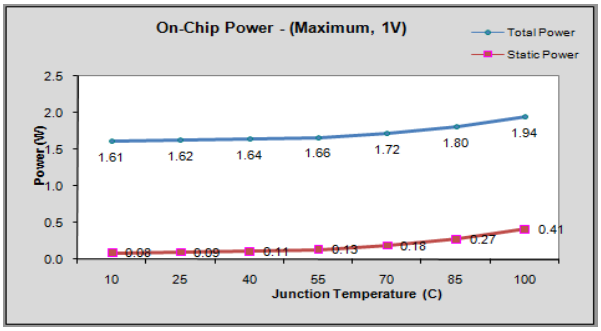


Figure 11: Power Consumption of Ripple Carry Adder using MHNG Gates

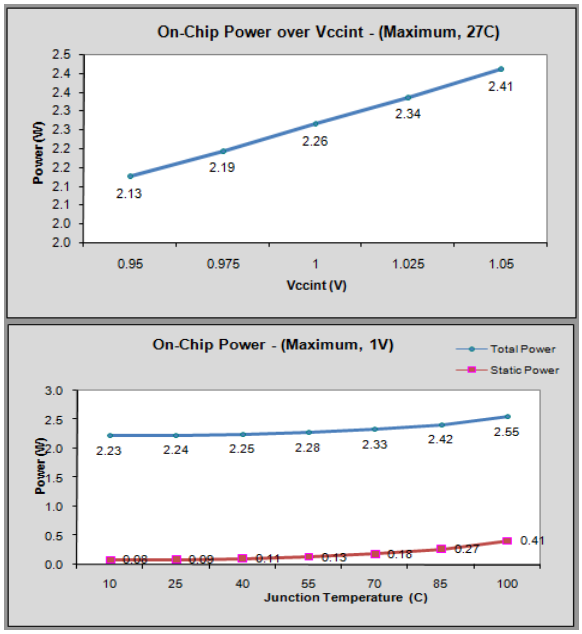


Figure 12: Power Consumption of Carry Skip Adder Using MTSG,PG and FRG Gates

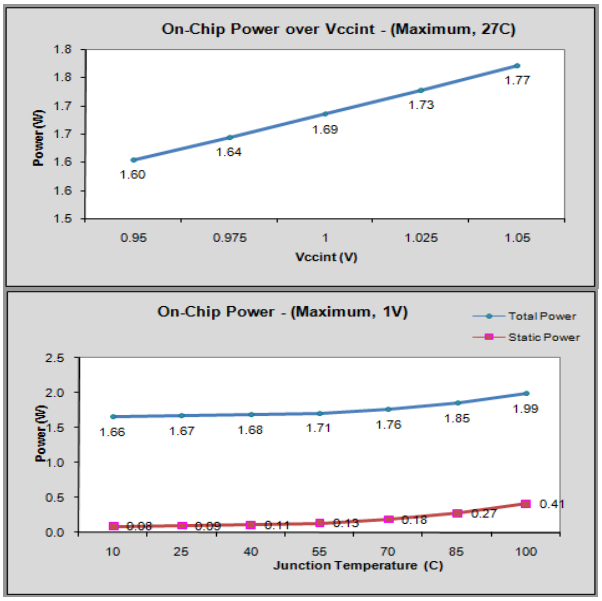


Figure 13: Power Consumption of Carry Skip Adder using MTSG,PG and MFRG Gates

The proposed reversible ripple carry adder and carry skip adder circuits are more efficient than the existing circuits presented in [7] and [10]. Evaluation of proposed circuit can be comprehended easily with the help of the comparative results in Table 1. The device utilization of ripple carry adder and carry skip adder using different reversible logic gates is shown in Table 2. Therefore, the proposed reversible ripple carry adder and carry skip adder circuits are better than the existing circuits in terms of complexity. One of the other major constrains in designing a reversible logic circuit is less quantum cost.

## IV. CONCLUSION

In this paper, we presented reversible ripple carry adder and carry skip adder circuit using MTSG gates, MHNG gates, and MFRG gates. Table I demonstrates that the proposed reversible ripple carry adder and carry skip adder circuits are better than the existing designs in terms of hardware complexity and quantum cost. Our proposed reversible ripple carry adder and carry skip adder circuits can be applied to the design of complex systems in nanotechnology.

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